CLAIMS

WHAT IS CLAIMED:

1. A semiconductor device comprising:

an insulating substrate;

a semiconductor layer formed on said insulating substrate;

a P-doped region formed in said semiconductor layer;

an N-doped region formed in said semiconductor layer;

a PN-junction formed between said P-doped region and said N-doped region; and

an insulating region formed on said semiconductor layer and covering said PN-junction, said insulating region having a thickness that is configured to substantially avoid a capacitive coupling to said PN-junction.

2. The semiconductor device of claim 1, wherein said P-doped region and said N-doped region are arranged substantially in a side-by-side configuration.

3. The semiconductor device of claim 1, wherein one of said P-doped region and said N-doped region is arranged to at least partially enclose the other one of the P-doped region and the N-doped region.

4. The semiconductor device of claim 1, wherein said semiconductor layer has a thickness in the range of approximately 0.05-0.1μm.

5. The semiconductor device of claim 1, further comprising a first contact plug, connecting to said P-doped region, and a second contact plug, connecting to said N-doped region.

6. The semiconductor device of claim 5, wherein a space formed between said first and second contact plugs is substantially filled with insulating material including said insulating region.

7. The semiconductor device of claim 1, further comprising a first metal silicide region in said P-doped region and a second silicide region in said N-doped region.

8. A diode structure in an SOI device, comprising:

a P-doped region and an N-doped region arranged to form a PN-junction;

a first silicide region formed in said P-doped region;

a second silicide region formed in said N-doped region;

a first contact plug connecting to said first silicide region;

a second contact plug connecting to said second silicide region; and

an insulating material formed between said first and second contact plugs so as to substantially fill a space therebetween.

9. The diode structure of claim 8, wherein said P-doped region and said N-doped region are arranged substantially in a side-by-side configuration.

10. The diode structure of claim 8, wherein one of said P-doped region and said N-doped region is arranged to at least partially enclose the other one of the P-doped region and the N-doped region.

11. A method, comprising:

forming a dielectric mask region above a semiconductor layer formed on an insulating substrate; and

forming a P-doped region and an N-doped region in said semiconductor layer using said dielectric mask region to create a PN-junction between the P-doped region and the N-doped region below said dielectric mask region.

12. The method of claim 11, further comprising forming silicide regions in said P-doped and N-doped regions, wherein said dielectric mask region prevents a short between the P-doped region and the N-doped region.

13. The method of claim 11, further comprising forming an insulating layer on said semiconductor layer, wherein said dielectric mask region is formed on said insulating layer.

14. The method of claim 11, further comprising adjusting a width of said dielectric mask region so as to control a dopant gradient towards said PN-junction.

15. The method of claim 14, wherein said width is in the range of approximately 0.03-0.2 μm.

16. The method of claim 11, wherein forming said P-doped region and said N-doped region includes forming a resist mask to cover a first portion and expose a second portion of said semiconductor layer and to partially cover said dielectric mask region.

17. The method of claim 16, further comprising implanting N-type dopants into said second portion to form the N-doped region.

18. The method of claim 17, further including forming a second resist mask to cover said second portion and expose said first portion of said semiconductor layer and to partially cover said dielectric mask region.

19. The method of claim 18, further comprising implanting P-type dopants into said first portion to form the P-doped region.

20. The method of claim 11, further comprising forming a first contact plug, connecting to said P-doped region, and forming a second contact plug, connecting to said N-doped region.

21. The method of claim 11, wherein said P-doped region and said N-doped region are arranged in a side-by-side configuration.

22. The method of claim 11, wherein one of said P-doped region and said N-doped region is arranged to at least partially enclose the other one of said P-doped region and said N-doped region.

23. The method of claim 11, further comprising forming a transistor structure in said semiconductor layer.

24. The method of claim 23, further comprising forming a halo implantation mask that at least covers a first portion and a second portion of said semiconductor layer prior to forming said P-doped region and said N-doped region in said first and second portions, respectively.